a marked up version has not been changed relative to the immediate prior version, except that marked up versions are not being supplied for any added claim or canceled claim.

CLAIMS

1. (Amended) Integrated circuitry comprising a capacitor comprising a first capacitor electrode, a second capacitor electrode and a high K capacitor dielectric region received therebetween; the high K capacitor dielectric region comprising a high K substantially amorphous material layer and a high K substantially crystalline material layer, the high K substantially amorphous material and the high K substantially crystalline material constituting different chemical compositions, the high K substantially crystalline material being received over the high K substantially amorphous material; and

wherein the high K substantially crystalline material layer is at least 70% crystalline and less than 98% crystalline.

4. The integrated circuitry of claim 1 wherein at least one of the first and second electrodes comprises elemental metal, metal alloy, conductive metal oxides, or mixtures thereof.

5. The integrated circuitry of claim 1 wherein at least one of the high K substantially amorphous material layer and the high K substantially crystalline material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

6. The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

7. The integrated circuitry of claim 6 wherein the high K substantially amorphous material layer contacts only one of the first capacitor electrode and the second capacitor electrode.

8. The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer contacts one of the first and second capacitor electrodes and the high K substantially crystalline material layer contacts the other of the first and second capacitor electrodes.

9. The integrated circuitry of claim 1 wherein the high K capacitor dielectric region is the only capacitor dielectric region received between the first and second capacitor electrodes, and consists essentially of the high K substantially amorphous material layer and the high K substantially crystalline material layer.

10. The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer is at least 98% amorphous, and the high K substantially crystalline material layer is at least 98% crystalline.

11. The integrated circuitry of claim 1 comprising a semiconductor substrate, the capacitor being received at least partially over the semiconductor substrate, the high K substantially amorphous material layer being received between the semiconductor substrate and the high K substantially crystalline material layer.

12. The integrated circuitry of claim 11 wherein the semiconductor substrate comprises bulk monocrystalline silicon.

13. The integrated circuitry of claim 11 wherein at least one of the high K substantially amorphous material layer and the high K substantially crystalline material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

14. The integrated circuitry of claim 11 wherein the high K substantially amorphous material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

15. The integrated circuitry of claim 1 comprising a semiconductor substrate, the capacitor being received at least partially over the semiconductor substrate, the high K substantially amorphous material layer being received between the semiconductor substrate and the high K substantially crystalline material layer.

16. The integrated circuitry of claim 15 wherein the semiconductor substrate comprising bulk monocrystalline silicon.

56. The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer is at least 70% amorphous.

57. The integrated circuitry of claim 1 further comprising a substrate supporting the first and second capacitor electrodes, and an insulative layer intermediate the substrate and the first and second capacitor electrodes.

58. The integrated circuitry of claim 57 wherein the insulative layer comprises an oxide layer.

59. The integrated circuitry of claim 57 wherein the insulative layer comprises silicon dioxide.

60. The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer comprises a thickness in a range of about 20 Ångstroms to about 250 Ångstroms.

61. The integrated circuitry of claim 1 wherein the high K substantially crystalline material layer comprises a thickness in a range of about 20 Ångstroms to about 90 Ångstroms.

62. The integrated circuitry of claim 1 wherein the high K capacitor dielectric region comprises a thickness in a range of about 40 Ångstroms to about 500 Ångstroms.

New Claims

63. (New) Integrated circuitry comprising:

a substrate having insulative material formed over the substrate; and

an opening formed in the insulative material; and

a capacitor comprising:

a first electrode layer formed within the opening;

a high K dielectric layer formed over the first electrode layer and within the opening; and

a second electrode layer formed over the high K dielectric layer.

64. (New) The integrated circuitry of claim 63 wherein the high K dielectric layer has at least a portion comprising crystalline material.

65. (New) The integrated circuitry of claim 63 wherein the high K dielectric layer has at least a portion comprising amorphous material.

66. (New) The integrated circuitry of claim 63 wherein the high K dielectric layer comprises a portion of amorphous material and a portion of crystalline material.

67. (New) The integrated circuitry of claim 63 wherein the high K dielectric layer comprises an amorphous layer adjacent the first electrode layer and a crystalline layer adjacent the second electrode layer.

68. (New) The integrated circuitry of claim 63 wherein the high K dielectric layer comprises a crystalline layer adjacent the first electrode layer and an amorphous layer adjacent the second electrode layer.

69. (New) The integrated circuitry of claim 63 wherein the high K dielectric layer has at least a portion comprising less than or equal to 98% crystalline material.

70. (New) The integrated circuitry of claim 63 wherein the high K dielectric layer has at least a portion comprising less than or equal to 98% amorphous material.

71. (New) The integrated circuitry of claim 63 wherein the opening comprises a trench.

72. (New) The integrated circuitry of claim 63 wherein the second electrode layer is formed within the opening.